ABSTRACT OF THE DISCLOSURE

A frame memory device capable of processing graphic data at high speed so as to reduce a burden to be imposed on a processor in a portable terminal of a limited size is disclosed. The frame memory device includes a number of memory cells aligned in a matrix form, and range selectable row/column address decoders capable of designating row/column addresses of a desired range by two addresses, to thereby select a number of memory cells of a desired range all at a time and write data in the selected memory cells,